Detectors for New Sources and New Science

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March 2, 2010
Outline

- Characteristics of new x-ray sources.
- Some detector characteristics.
- Some detectors under development or in use.
- What is to be done next? (i.e. what needs can we anticipate?)

Disclaimer: Talk will have bias toward 2-D imaging CMOS based detectors
New Sources

- New sources: peak brilliance $10^9$ higher than 3rd generation synchrotrons.
- Complete game changer for possible science and demands on detectors.
New Sources

[Spectral Brightness graph showing different energy (eV) sources including ERL 18 mm Delta (25m), helical mode, ERL 19mm Delta (5m), NSLS-II U20 (3m), and APS A (2.4m).]
Characteristics of Detectors
(High-level considerations)

- Energy range and efficiency.
- Signal-to-ratio.
- Saturation (or full well).
- Speed (frame rate – sustained and burst)
- Pixel size.
- Number of pixels, size of array.
- Active area.
- Packaging.
- Bump-bonding, 3-D technology.
- Detector control.
- Data Storage and analysis.
- Interface between source and detector (e.g. synchronization).
- Calibration procedures (anticipate required hardware).
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Detectors are complex and decisions/trade-offs are made at the very early stages of design.
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- Window material
- Radiation Hardness
- Single x-ray signal (e-/photon)
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- Front-end electronic design.
- Headroom.
- Noise
- Dynamic Range
- In-pixel Storage?
- 'Count-rate'?
- Process Technology? Die Size?
- Experiment geometry/solid angle?
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- Who are the vendors? What is the available technology? Where will the detector go? Who will look at/analyze the data? Constraints on the housing? How is the detector cooled? What is needed to maintain calibration? Are there special requirements? What is the cost? Is there a power budget? How do you get the data off the detector? Where is it stored?
Characteristics of Detectors
(High-level considerations)

The points:

• Lots of things to consider.
• Know the intended applications.
• Know where and how the detector will be used.
• Figure out the experimental requirements.
Exciting Days for Detectors

- Add pictures Pixel Array Detectors (shown: Medipix, Pilatus), pnCCDs, DEPFETs.

Medipix (1,2,3, TimePix)  Pilatus

Photon counting
Pixel Array Detector
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Photon counting
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Will Not Talk About These
Pixel Array Detectors

- Application Specific Integrated Circuit.
Pixel Array Detectors

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Pixel Array Detectors

- Diode – mated to ASIC with individual pixel-level connections.
Pixel Array Detectors
Why Pixel Array Detectors (PADs)?

- Extremely flexible pixel level signal processing.
  - e.g. In-pixel analog storage, in-pixel gain control, in-pixel ADC.
- CMOS mature technology.
- Commercial processes used to make new detectors.
1. Photocurrent \( (I_{\text{sig}}) \) collects in the integrator.

2. The integrator output \( (V_{\text{out}}) \) slews towards ground.

3. When \( V_{\text{out}} < V_{\text{th}} \), the comparator activates a gated oscillator.

4. Each oscillator cycle removes a fixed quantity of charge \( (\Delta Q) \) from the integrator and increments an in-pixel counter \( (N_{\Delta Q}) \).
MMPAD

Flux limited.

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In-Pixel Storage

In-Pixel Storage

Used for high-speed radiography.
New Experiments
Coherent X-ray Imaging

One pulse, one measurement
Particle injection

10 fs pulse

Noisy diffraction pattern

Combine $10^5 - 10^7$ measurements

Classification  Averaging  Orientation  Reconstruction
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Classification

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Orientation

Reconstruction

LCLS CXI Detector
CXI Detector

Pixel Schematic: In-pixel ADC → all digital output, programmable multiple gain

ASICSs being assembled into full detector now.

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CXI Detector

- Each quadrant 758x758 pixels.
- Whole detector 1516 x 1516 pixels.
- Frame Rate 120Hz.
CXI Detector

- High gain single photon peaks.
- Charge conserved.
The European XFEL

Time structure: difference with “others”

Electron bunch trains; up to 3000 bunches in 600 $\mu$sec, repeated 10 times per second. Producing 100 fsec X-ray pulses (up to 30 000 bunches per second).

30 000 bunches/s but 99.4 ms (%) emptiness

X-ray photons 100 fs

FEL process

DESY Tuesday Seminar, 10 October 2006

Heinz Graafsma
The Adaptive Gain Integrating Pixel Detector (AGIPD)

**High dynamic range:**

**Dynamically gain switching system**

**Extremely fast readout (200ns):**

**Analogue pipeline storage**

For European XFEL
Definition of final design: End of 2010

**PSI/SLS - Villingen:** chip design; interconnect and module assembly

**Universität Bonn:** chip design

**Universität Hamburg:** radiation damage tests, “charge explosion” studies; and sensor design

**DESY:** chip design, interface and control electronics, mechanics, cooling; overall coordination

Large portion of slide taken from Heinz Graafsma Talk (CHESS, Dec. 2009)
The Adaptive Gain Integrating Pixel Detector (AGIPD)

64 x 64 pixels

1k x 1k (2k x 2k)

~ 2mm

~ 220 mm

Large portion of slide taken from Heinz Graafsma Talk (CHESS, Dec. 2009)
The Adaptive Gain Integrating Pixel Detector (AGIPD)

Integration of charge and gain switching.

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Large portion of slide taken from Heinz Graafsma Talk (CHESS, Dec. 2009)
Large Pixel Detector (LPD)

Diode

Primary Integration Stage

Three Different Secondary Stages With different gains

Lots of storage capacitors, 3 caps for each frame.

Large portion of slide taken from Heinz Graafsma Talk (CHESS, Dec. 2009)
Where is the technology going?

- Vertical integration of CMOS.
  - Through silicon vias (TSVs) – good for eliminating dead space, power connections, analog and digital signals, thermal, increasing functionality per unit area.

- Smaller feature size, lower voltage, concentration on digital electronics.
  - Smaller feature size good if you want smaller pixels, more pixel-level functionality.
  - Lower voltage – not so good for analog design.
3D Integration

Possible 3D Vendors:
Tezzaron, Ziptronics, RTI, and more.

Groups Looking at 3D CMOS integration:
Fermilab.

Image Source: Samsung
MCP: Multi-Chip Package, WSP: Wafer-Level Stacked Package

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That's Great Now What?

- Q: What are the demands on detectors?
- A: Large area, fast frame rates, little dead space, able to handle very high instantaneous count rates, more pixels, single photon sensitivity.
Huge Amounts of Data

- Example: LCLS CXI PAD:

\[
(185 \times 194 \frac{\text{pixels}}{\text{ASIC}})(64 \text{ ASIC})(14 \frac{\text{bit}}{\text{pixel}})(120 \text{ Hz}) = 3.86 \text{ Gbit/s}
\]

- continuously!

- Potentially 41 Tbytes/day.

- European XFEL – even more.
Detectors Need to be More Intelligent

- Algorithms to determine:
  - Is Data Valid.
  - Can Data be compressed?
  - Harness the power of digital processing in real time to determine if more data is needed.
Ideal Development Path?

- European Model: Teams of many research groups and universities working on one detector.
- American Model: Small independent groups.
Conclusions

- Compared to other detector technologies available, PADs offer an extremely flexible technological platform for detector development.

- Using commercial foundries with established CMOS processes is a relatively quick, low-risk path to developing detectors to meet scientific needs.

- Industry if moving toward vertical stacking of CMOS with through silicon vias. This is good!

- Increased demands on detectors makes things like in-pixel frame storage necessary with the present technologies.

- Increasing detector intelligence can be a solution to some future challenges.
Cornell Detector Group

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