ARD ILC
High Availability Electronics Development

Ray Larsen
May 26, 2011
Outline FY11 Program

- Standards Program
  - Lab-Industry Collaboration
  - Standards Progress
- Lab Infrastructure Development System
  - Industry Hardware
  - Software environment development
- SLAC Demonstration Projects
  - ILC RF station interlocks from VME to MicroTCA
  - RF demonstration goals for FY12
- Other SLAC projects, international collaboration
Standards Motivation

- ILC studies proved much higher availability of all subsystems required to reach even modest availability goal (85%)
- Then-new telecom platform standards ATCA, MicroTCA* offered potential solution adding extensions for physics
- Designed for A=0.99999 combining redundancy, hot-swap, Intelligent Platform Management Interface (IPMI)
- Advanced serial multi-gigabit backplanes eliminates single-point-of-failure parallel buses (e.g. CAMAC, VME)
- Orders of magnitude higher BW, throughput available

*ATCA- Advanced Telecom Computer Architecture
Method

- Form collaboration between interested labs and *Open Source* industry standards group PICMG*
- Develop physics standards under industry umbrella simultaneously developing industry-supported infrastructure
- Maintain compatibility with existing xTCA products meeting PICMG interoperability tests for broadest market reach outside of physics world

*PCI Industrial Computer Manufacturers’ Group*
Program Goals FY10-12*

- Extend PICMG Standards for physics - hardware, software, firmware
- Develop COTS** availability of key infrastructure components
- Demonstrate interoperability of lab, industry components
- Demonstrate technical and economic viability via example lab applications
- Establish inter-lab collaborations to share development costs

*Supported by ILC key technology development funds
**Commercial Off-The-Shelf
Standards for Physics Goals

- Extend features of new Telecom standard to accommodate physics applications in both controls and detectors
  - Expand analog-digital I/O via Rear Transition Modules
  - Preserve gigabit analog bandwidth through I/O connectors.
  - Add precision clocking (timing and triggering) features
  - Create *interoperable* designs
PICMG xTCA for Physics

- PICMG Technical Committees established June 2009
  - **Hardware**: IO, Triggering and Precision Timing
    - Chair Robert Downing, under contract to SLAC
  - **Software**: Architectures and Protocols
    - Chair Stefan Simrock, formerly DESY and now ITER
  - **Coordinating Committee**: Steering Committee for current, future SOWs and Tasks
    - Chair: Ray Larsen
  - Typical standard development takes ~2 years through final ballot, approval
Physics Standards Progress 2009-11

- **MicroTCA**
  - *MTCA.4* Dual Star 12-slot crate, AMC module, μRTM Rear Transition Module with IPMI and backplane timing distribution standard out for final approval

- **ATCA**
  - *PICMG3.8* Rear Transition Module I/O and management standard submitted for comment
  - Backplane Clocking Distribution Guideline Reference Document draft in development
Physics Standards Progress 2

- Software Architecture & Protocols
  - Extensive Roadmap developed with ~7 major tasks
  - Guidelines on *Standard Process Model* and *Standard Device Model* in draft form
- Other:
  - Virtual device APIs to EPICS translation interface
  - Enterprise-wide timing, IPMI management
  - Reference implementations for novices
  - Low latency protocols
  - Redundancy and failover management
  - In-field SW-FW fast updates, etc.
HWG Work Products

MicroTCA™
PICMG® Specification MTCA.x
R 1.0 Draft 0.9xg
MicroTCA Enhancements for Rear I/O and Precision Timing
21 April 2011
For Member Review Only - Do Not Claim Compliance To or Distribute This Draft Specification

AdvancedTCA®
PICMG® 3.8
R1.0 D0.9xc
AdvancedTCA Rear Transition Module Zone 3A
3 May 2011

μTCA®
Open Modular Computing Specifications

PICMG Reference Document
CGT 1.0 D0.1a (place holder)
Overview of Clocks, Gates & Triggers for xTCA Physics
24 May 2011

Open Modular Computing Specifications

SLAC NATIONAL ACCELERATOR LABORATORY
5/25/2011
ARD ILC HA Electronics R&D - RLarsen
SWG Guidelines Progress

xTCA for Physics
Standard Device Model Design Guide

Guidelines for designing I/O access software for xTCA-based physics systems

May 23, 2011
Rev. 0.0.2

This design guide is not a specification; it contains additional detail information but does not replace any applicable Fermilab xTCA for Physics specifications.

For complete guidelines on the design of xTCA for Physics compliant boards and systems, refer also to the full specification – do not use this design guide as the only reference for any design decisions.

xTCA for Physics
Standard Process Model Design Guide

Guidelines for designing multi-threaded software for xTCA-based physics systems

October 6, 2010
Rev. 00.4

This design guide is not a specification; it contains additional detail information but does not replace any applicable Fermilab xTCA for Physics specifications.

For complete guidelines on the design of xTCA for Physics compliant boards and systems, refer also to the full specification – do not use this design guide as the only reference for any design decisions.
Lab Development Infrastructure

- Through standards collaboration industry developed first crates & basic boards
- Physics board space ~4x a “single wide” standard AMC* board including Rear Transition Module
- Architecture is AMC board with complex FPGA computer in front, simpler analog signal conditioning and calibration on μRTM designed for different applications
MTCA.4 Prototype Chassis, AMC, µRTM

6-Slot shelf  RTM I/O Connector

Front Panels  2-wide AMC  Rear I/O Panels

2-wide RTM  Backplane Edge Connector
MTCA 12-Slot Shelf & Modules

12 Slot Crate & Front-Rear Fan Tray (Schroff)

6 Slot Crate w/ AMC & RTM (Schroff)

May 2010, Lisbon Workshop
## MTCA.4 Timing, Vector Sum, Intlk Bus

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</table>

**Common**:
- 1GbE
- SAS/SATA

**Fat Pipe**:
- PCIe or SRO
- 1GbE/SRIO

**Extended Options**:
- Point-2-point links
- TCLKC TCLKD
- Triggers, Clocks, Interlocks

**Clocks**:
- Clk 1
- Clk 2
- Clk 3

**Vector, Interlock Sums**

**Parallel Triggers**

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5/25/2011 ARD ILC HA Electronics R&D - RLarsen

15
Precision Timing Distribution

Distribution of clock, trigger, time stamp (event #) from a central timing via the backplane to AMCs

1.3GHz/12 = 108MHz clock with encoded data: Triggers, timestamps, ...

1.3GHz clock with encoded data, drift compensated

Central Timing Generator

MCH
- Clk 2 crosspoint switch
- Clk 1 crosspoint switch

Backplane

AMC: Timing

AMC: ADC

μTCA Shelf

Kay Rehlich, DESY, 16.2.2010
SLAC Development Platform

- 6-Slot Prototype Shelf w/ MCH, Processor, Interim Timing System, power module, built-in fans
- Event Receiver (EVR) on double MTCA PMC Adapter
- Shelf non-redundant
- All rear I/O access
Timing AMC (University of Stockholm)

- Fiber optic links w/ drift compensation
- ps stability
- AMC module is receiver and transmitter
- Clock, trigger and event distribution

SLAC has unit in hand for testing
Reference Design complete w/ supporting FW-SW environment enables engineers to focus on payload design w/ power, IPMI basic infrastructure standardized

- Double-wide plus RTM provides excellent analog space, ground noise control, crosstalk
- AMC space fully backward compatible with industry single-wide designs
Applications: BPMs, Toroids, Gated ADCs

**AMC 1**
- FAST ADC
- 4 CH 16 BIT 119 MSPS (180 MSPS MAX)

(Struck, Vadatech, Libera)

**RTM 1**
- STRIPLINE BPM (2 TYPES)
- SIGNAL CONDITIONING, FILTERING & CALIBRATION

**RTM 2**
- TOROID (2 TYPES)
- SIGNAL CONDITIONING & CALIBRATION

**RTM 2**
- GATED ADC SIGNAL CONDITIONING (GADC)

**Strategy:**
- Contract with Industry to provide key generic complex AMC modules
- Develop 2 or more sources
- Encourage multiple labs to collaborate on specifications
Applications: LLRF System, Feedback Apps

AMC 2
FAST ADC
10 CH 16 BIT 119 MSPS
2 CH DAC 238 MSPS

RF FREQUENCY GENERATION
LOCAL OSCILLATOR (LO)
SAMPLING CLOCKS
8 CH DOWNCONVERTER

2856 MHZ
REF IN

RTM-3
25 MHZ IF SIGNAL PASSTHROUGH
DAC OUTPUT TO RF AMP

I/O CNTRL
IF SIGS
DAC OUT

RTM-3
GENERIC FAST
SIGNAL CONDITIONING UP TO 10
CH ANALOG IN, 2 CH DAC OUT

(Struck, Vadatech, I-Tech)
Applications: Industry Pack Adapter

AMC 3
3-INDUSTRY PACK (IP)
ADAPTER FOR PHYSICS
BACKPLANE

1-3
INDUSTRY
PACKS

RTM 4
BLEN PROFILE MONITOR
GENERIC 3 IP 1/0
ADAPTER, SCSI PORT,
IPMI PASSTHOUGH

RTM 4
VACUUM GAUGE
READOUT, REMOTE
WAKEUP

RTM 4
VACU-ION PUMP
CONTROLLER
INTERFACE

RTM 4
WIRE SCANNER MOVERS
HYTEK IP DESIGN
PORT FW, SW FROM
XSTG DESIGN

(TEWS, Vadatech)
High BW Frame Grabber PMC Adapter

- AMC 4
  PMC ADAPTER
- RTM 5
  SIMPLE INTERFACE
  PASSTHROUGH FOR PMC
  E.G. PROFILE MONITOR
  HIGH DATA BW FAST FRAME GRABBER
- GENERIC ADAPTER E.G. VADATECH, TEWS
- FIBER OPTIC MULTI- GIGABIT LINKS
- STANDARD PMC BOARD
- (TEWS, Vadatech)

(Technical diagram illustrating the components and connections of a high bandwidth frame grabber PMC adapter.)
MTCA.4 New Industry Adaptations

- Fast 10 Ch ADC-DAC (Struck, Vadatech)
- Generic FPGA Module (TEWS)
- Generic Industry-Pack Module (TEWS, Vadatech, Hytec)
Struck SIS 8300 RF Digitizer

Controls Upgrade Implementation

RTM Connector

AMC Connector

10 Ch 16 bit 125 MSPS
2 Ch 16 bit DAC output
Virtex 5 FPGA

16 Bit 125 MSPS ADC-DAC ported from VME product
Strück ADC-DAC (L) with RTM (R)
FPGA, Fast ADC in development

Generic FPGA, fast 16 bit ADC-DAC designs being ported to MTCA.4
SLAC μRTM Modules in Progress

- **RF interface** to fast feedback MicroTCA ADC-DAC
  - IPMI managed RTM, all rear IO, hot swap
  - Extension of IPMI to RF front end chassis
  - Mates to Struck, Vadatech 10 Ch ADC 2 Ch DAC 125 MSPS
- **Klystron-modulator interlocks** 16 Ch analog section
  - Mates to TEWS Spartan FPGA with optical links available to μRTM
  - Perform same functions as VME F3 board currently running ESB test stand
SLAC μRTM Modules 2

- Stripline BPM Conditioning, Calibration
  - Mated to Struck or Vadatech ADC will be able to replace large pizza-box units in LCLS
  - Eliminate several racks, large network cable plant which becomes imbedded in MicroTCA switched backplane
Stripline BPM Map to MTCA.4

Filter & Calibration Section

To/From ADC-DAC

On ADC-DAC AMC
Schedule for FY11

- Schedule calls for completion new interlocks ESB hardware, firmware by end FY11 (D. Brown)
  - TEWS FPGA module order in process for delivery first unit by Aug 15, 4 units by Sept 15
  - Will reuse significant portion of new FW developed for MKSUII chassis (J. Olsen)
  - EPICS SW may be late due to pressures of other ARD work in late summer
## Task Name

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<td>FY11 ARB ATCA PROGRAM</td>
<td>6%</td>
<td>136 hours</td>
<td>127 days</td>
<td>Mon 5/2/11</td>
<td>Wed 10/26/11</td>
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<tr>
<td>Management</td>
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<td>150 hours</td>
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<td>Complete/Approve MTCA specification</td>
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<td>Complete/Approve PAMO3.3 Specification</td>
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<td>22.7 hours</td>
<td>16.72 days</td>
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<td>Thu 6/23/11</td>
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<td>45.81 days</td>
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<td>44 hours</td>
<td>11.05 days</td>
<td>Mon 5/2/11</td>
<td>Fri 5/6/11</td>
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<td>Mon 5/2/11</td>
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<td>0%</td>
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<td>70 days</td>
<td>Mon 5/2/11</td>
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### Procure-Eval Chassis 6 slot
- 100% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Procure-Eval Chassis 12 slot
- 0% | 50 hours | 60 days | Mon 5/2/11 | Mon 5/2/11 |

### Procure-Eval MCH
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Procure-Eval Processor
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Procure-Eval Timing modules
- 0% | 220 hours | 70 days | Mon 5/2/11 | Fri 8/5/11 |

### Eval-2-wide AMC Adapter EVR (Micro Research) Module
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Eval-1-wide Stockholm Tx-Rx MTCA,4 Module
- 0% | 100 hours | 25 days | Mon 5/2/11 | Fri 7/8/11 |

### Demonstrate EVR code in MTCA,4 Tx-Rx Module
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Procure-Eval 2-wide Stockholm MTCA,4 Rx Module
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Demonstrate EVR code in 2-wide MTCA,4 Rx Module
- 0% | 0 hours | 0 days | Mon 5/2/11 | Mon 5/2/11 |

### Reference Board Designs (Document)

### FPGA Design Interface (RF)

### MTCA Interlock AMC purchase, RTM design

### Brown
- 0% | 1.0 hours | 2 days | Mon 5/2/11 | Tue 5/3/11 |

### Procure EMIS FPGA
- 0% | 0 hours | 75 days | Wed 5/4/11 | Tue 6/16/11 |

### RTM circuit design completion
- 0% | 0 hours | 20 days | Wed 5/4/11 | Tue 5/31/11 |

### Circuit Design Review Prep
- 0% | 8 hours | 2 days | Wed 6/4/11 | Thu 6/2/11 |

### Circuit Review
- 0% | 0 hours | 0 days | Thu 5/2/11 | Thu 5/2/11 |

### RTM layout
- 0% | 60 hours | 15 days | Fri 6/3/11 | Thu 6/23/11 |

### Board Design Review Prep
- 0% | 4 hours | 1 day | Fri 6/24/11 | Fri 6/24/11 |

### Board Test
- 0% | 4 hours | 1 day | Mon 6/27/11 | Mon 6/27/11 |

### Board Load
- 0% | 4 hours | 12.5 days | Wed 6/23/11 | Thu 7/14/11 |

### Generate 1st Cdl FPGA code (integrate MCTCA spec)
- 0% | 0 hours | 0 days | Thu 7/14/11 | Thu 7/20/11 |

### Module Testing - Bench
- 0% | 160 hours | 33 days | Wed 8/17/11 | Wed 9/28/11 |
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<td>168 hrs</td>
<td>36.33 days</td>
<td>Wed 8/17/11</td>
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<td>Bring up TBWS board</td>
<td>0%</td>
<td>40 hrs</td>
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<td>Requirements document</td>
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<td>8.33 days</td>
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## Budget EAC Summary

| 1111202 | SLAC Labor | 126 | 73 | 73 | 74 | 147 (20) |
| 1111202 | Shop Services | 204 | 117 | 117 | 100 | 217 (13) |
| 1111202 | M&S | 150 | 79 | 41 | 120 | 45.3 | 165 (15) |
| 1111202 | Travel | 10 | 1 | 1 | 4 | 5 | 5 |
| 1111202 | Allocated OH | 197 | 110 | 110 | 90 | 200 (2) |
| 1111202 | PrgmSuprt | 13 | 7 | 7 | 5 | 12 | 0 |
| 1111210 | Shop Services | 52 | 102 | 102 | 118 | 220 (168) |
| 1111210 | M&S | 40 | 0 | 0 | 25 | 25 | 15 |
| 1111210 | Allocated OH | 31 | 53 | 53 | 63 | 116 (85) |
| 1111210 | PrgmSuprt | 0 | 0 | 0 | 0 | 0 | 0 |

### Labor & SS to complete:

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*Split 74+100*
Plans for FY 12

- **Standards**
  - Complete hardware, software standards committee handoff to engineering division (assuming no ILC funding beyond FY12)
  - Add SLAC members to HW committee (already have 2 SLAC people on SW committee)
- **Instrument single channel of LLRF feedback and control on ILC 10 MW Test Station in ESB**
  - Obtain copy of DESY RF L-Band down-mixer design on RTM
  - Struck or Vadatech ADC-DAC
  - Develop controls intra-pulse feedback algorithm similar to ongoing effort for RF AIP
  - Imbed RF in same crate with interlock system
  - Conduct performance test and measurement program
Future Goals

• Collaborations are backbone of new standards development, implementation & commercialization

• Resources:
  • PICMG –Lab Committees (8 labs, 40+ companies)
    • CERN, DESY, FNAL, IHEP, IPFN, ITER, LBNL, SLAC
  • Lab collaborations for mutual support, design exchange (MOUs with DESY, ESSB, IPFN, LBNL...)
  • CERN Interest Group & Design Repository
    • Sharing of open source designs, website
  • Meetings and Workshops
    • Yearly xTCA for Physics workshops at IEEE conferences since 2007
    • Annual ATCA Summit meetings with Industry, telecom and non-telecom customer base
    • New short courses under discussion for October 2011 NSS-MIC, May 2012 Real Time Controls at LBNL